UNITRODE

UCC1809-1/-2
UCC2809-1/-2
UCC3809-1/-2

Economy Primary Side Controller

PRELIMINARY

FEATURES

- User Programmable Soft Start With Active Low Shutdown
- User Programmable Maximum Duty Cycle
- Accessible 5V Reference
- Undervoltage Lockout
- Operation to 1MHz
- 0.4A Source/0.6A Sink FET Driver
- Low 100µA Startup Current

DESCRIPTION

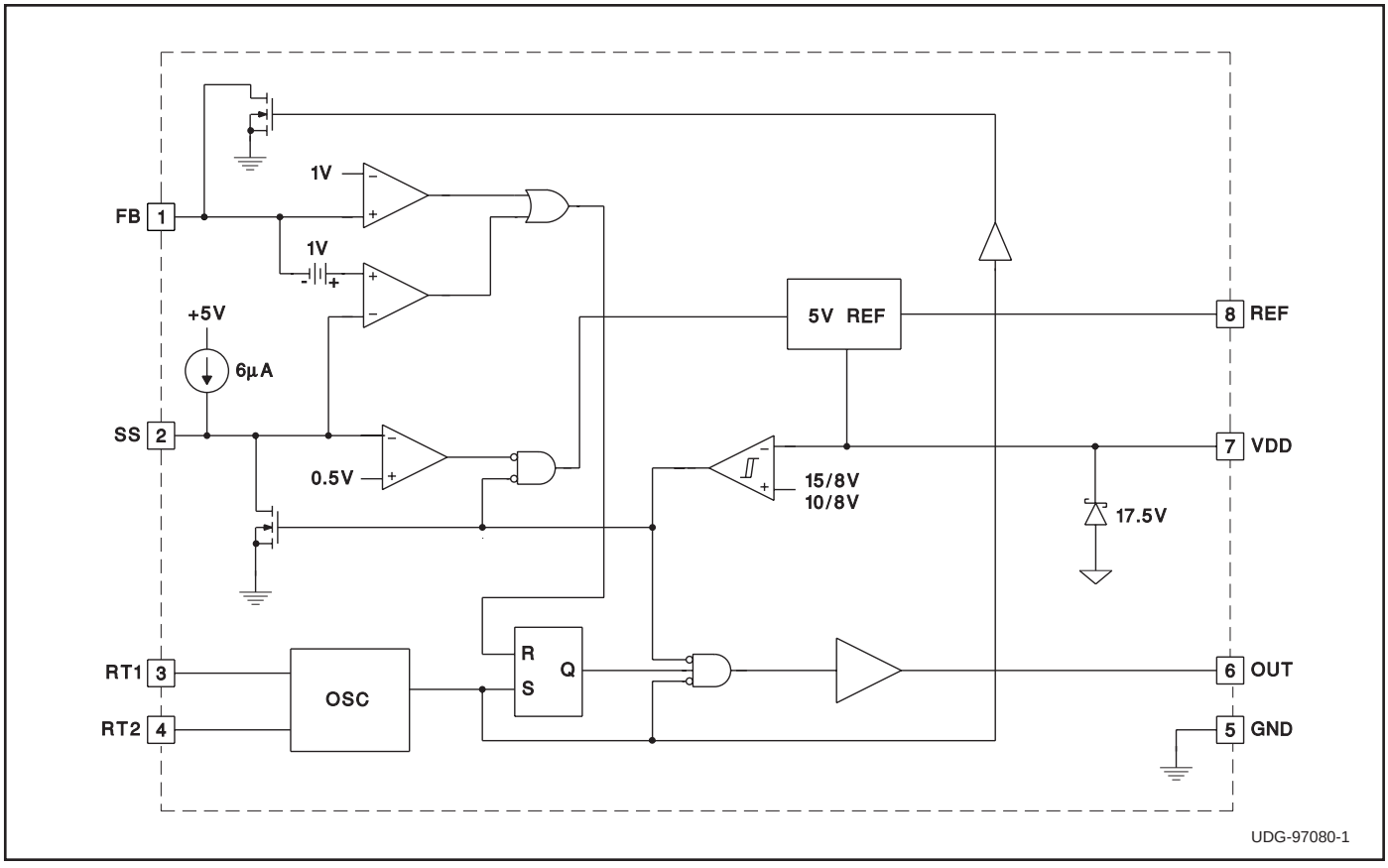
The UCC3809 family of BCDMOS economy low power integrated circuits contains all the control and drive circuitry required for off-line and isolated DC-to-DC fixed frequency current mode switching power supplies with minimal external parts count. Internally implemented circuits include undervoltage lockout featuring startup current less than 100µA, a user accessible voltage reference, logic to ensure latched operation, a PWM comparator, and a totem pole output stage to sink or source peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3809 family also features full cycle soft start.

The family has UVLO thresholds and hysteresis levels for off-line and DC-to-DC systems as shown in the table below.

PART NUMBER	TURN ON THRESHOLD	TURN OFF THRESHOLD
UCCX809-1	10V	8V
UCCX809-2	15V	8V

BLOCK DIAGRAM



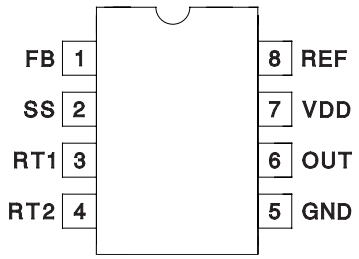
ABSOLUTE MAXIMUM RATINGS

VDD 19V
I_{VDD} 25mA
I_{OUT} (tpw < 1µs and Duty Cycle < 10%) . . . . . –0.4A to 0.6A
RT1, RT2, SS . . . . . -0.3V to REF + 0.3V
I_{REF} . . . . . –15mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8 (Top View)
D, N and J Packages



	Temperature Range	Available Packages
UCC1809-X	–55°C to +125°C	J
UCC2809-X	–40°C to +85°C	N, D, J
UCC3809-X	0°C to +70°C	N, D

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Section					
VDD Clamp	I_{VDD} = 10mA	16	17.5	19	V
I_{VDD}	No Load		600	900	µA
I_{VDD} Starting				100	µA
Undervoltage Lockout Section					
Start Threshold (UCCx809-1)		9.5	10	10.5	V
UVLO Hysteresis (UCCx809-1)		1.8	2		V
Start Threshold (UCCx809-2)		14.2	15	15.8	V
UVLO Hysteresis (UCCx809-2)		6.0	7		V
Voltage Reference Section					
Output Voltage	I_{REF} = 0mA	4.75	5	5.25	V
Line Regulation	VDD = 10V to 15V		2		mV
Load Regulation	I_{REF} = 0mA to 5mA		2		mV
Comparator Section					
I_{FB}	Output Off		–100		nA
Comparator Threshold		0.9	0.95	1	V
OUT Propagation Delay (No Load)	V_{FB} = 0.8V to 1.2V at Tr = 10ns		50	100	ns
Soft Start Section					
I_{SS}	VDD = 16v, V_{SS} = 0V	–3	–6	–16	µA
V_{SS} Low	VDD = 7.5V, I_{SS} = 200µA			0.2	V
Shutdown Threshold		0.46	0.5	0.54	V
Oscillator Section					
Frequency	RT1 = 10k, RT2 = 4.32k, CT = 1nF	90	100	110	kHz
Frequency Change with Voltage	VDD = 10V to 15V		0.1		%/V
C_T Peak Voltage			3.33		V
C_T Valley Voltage			1.67		V
C_T Peak to Peak Voltage		1.54	1.67	1.80	V
Output Section					
Output V_{SAT} Low	I_{OUT} = 100mA (dc)		0.8	1.5	V
Output V_{SAT} High	I_{OUT} = –40mA (dc), VDD – OUT		0.8	1.5	V
Output Low Voltage During UVLO	I_{OUT} = 20mA (dc)			1.5	V
Minimum Duty Cycle	V_{FB} = 2V		0		%
Maximum Duty Cycle			70		%
Rise Time	C_{OUT} = 1nF		35		ns
Fall Time	C_{OUT} = 1nF		18		ns

PIN DESCRIPTIONS

FB: This pin is the summing node for current sense feedback, voltage sense feedback (by opto coupler) and slope compensation. Slope compensation is derived from the rising voltage at the timing capacitor and can be buffered with an external small signal NPN transistor. External high frequency filter capacitance applied from this node to GND is discharged by an internal 250Ω on resistance NMOS FET during PWM off time and offers effective leading edge blanking set by the RC time constant of the feed back resistance from current sense resistor to FB input and the high frequency filter capacitor capacitance at this node to GND.

GND: Reference ground and power ground for all functions.

OUT: This pin is the high current power driver output.

REF: The internal 5V reference output. This reference is buffered and is available on the REF pin. REF should be bypassed with a 0.47µF ceramic capacitor.

RT1: This pin connects to timing resistor RT1 and controls the positive ramp time of the internal oscillator (Tr = 0.69 • RT1 • C_T). The positive threshold of the internal oscillator is sensed through inactive timing resistor RT2 which connects to pin RT2 and timing capacitor CT.

RT2: This pin connects to timing resistor RT2 and controls the negative ramp time of the internal oscillator (Tf = 0.69 • RT2 • C_T). The negative threshold of the internal oscillator is sensed through inactive timing resistor RT1 which connects to pin RT1 and timing capacitor C_T.

SS: This pin serves two functions. The soft start timing capacitor connects to SS and is charged by an internal 6µA current source. Under normal soft start SS is discharged to at least 0.4V and then ramps positive to 1V during which time the output driver is held low. As SS charges from 1V to 2V soft start is implemented by an increasing output duty cycle. If SS is taken below 0.5V, the output driver is inhibited and held low. The user accessible 5V voltage reference also goes low and I_{VDD} < 100µA.

VDD: The power input connection for this device. This pin is shunt regulated at 17.5V which is sufficiently below the voltage rating of the DMOS output driver stage. VDD should be bypassed with a 1µF ceramic capacitor.

APPLICATION DIAGRAM

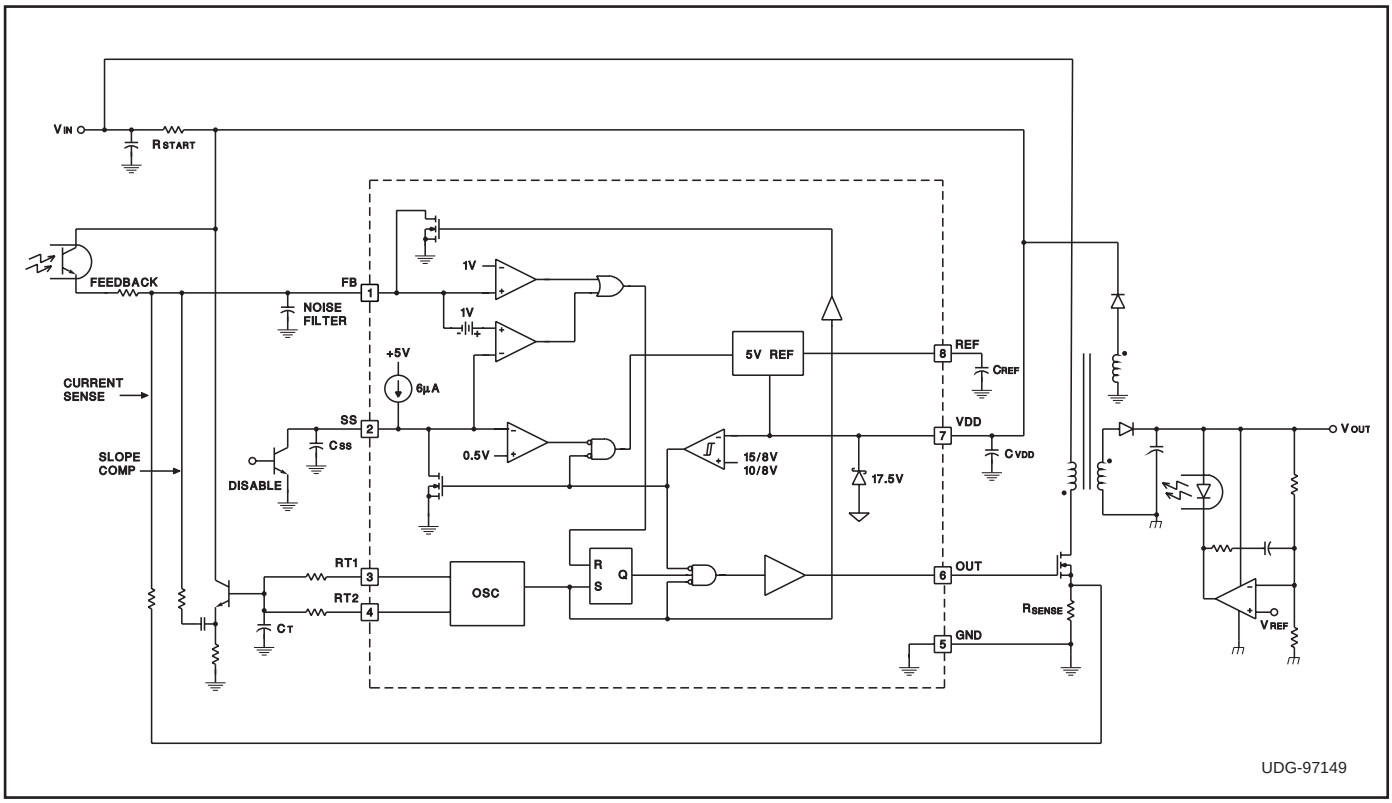


Figure 1. Typical Appliction Diagram

Figure 1 shows a typical isolated flyback converter utilizing the UCC3809. Note that the capacitors CREF and CVDD are local decoupling capacitors for the reference and IC input voltage, respectively. Both capacitors should be low ESR and ESL ceramic, placed as close to the IC pins as possible, and returned directly to the ground pin of the chip for best stability. VREF provides the internal bias to many of the IC functions and CREF should be at least 0.47µF to prevent VREF from drooping.

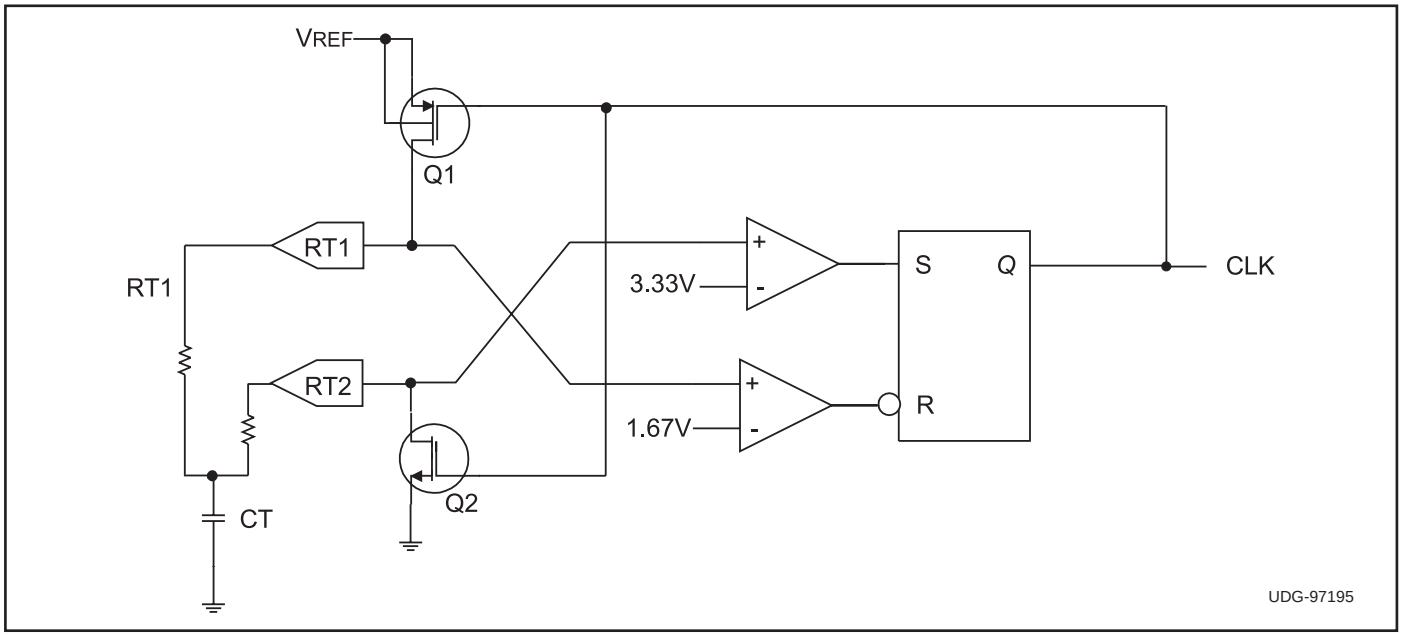


Figure 2. UCC3809 Oscillator

APPLICATION INFORMATION

FB PIN

The basic premise of the UCC3809 is that the voltage sense feedback signal originates from an optocoupler that is modulated by an external error amplifier located on the secondary side. This signal is summed with the current sense signal and any slope compensation at the FB pin and compared to a 1V threshold, as shown in the typical application circuit in Figure 1. Crossing this 1V threshold resets the PWM latch and modulates the output driver on-time much like the current sense comparator used in the UC3842. In the absence of a FB signal, the output will follow the programmed maximum on-time of the oscillator.

When adding slope compensation, it is important to use a small capacitor to AC couple the oscillator waveform before summing this signal into the FB pin. By correctly selecting the emitter resistor of the optocoupler, the voltage sense signal can force the FB node to exceed the 1V threshold when the output that is being compared exceeds a desired level. Doing so drives the UCC3809 to zero percent duty cycle.

OSCILLATOR

The following equation sets the oscillator frequency:

$$F_{OSC} = (0.69 \bullet CT \bullet (RT1 + RT2))^{-1}$$

$$D_{MAX} = 0.69 \bullet RT1 \bullet CT \bullet F_{OSC}$$

When Q1 is on, CT charges via the Rdson of Q1 and RT1. During this charging process, the voltage of CT is sensed through RT2. Crossing the upper threshold (set at 2/3 VREF or 3.33V for a typical 5.0V reference) sets the CLK signal high, turning off Q1 and turning on Q2. CT now discharges through RT2 and the Rdson of Q2. CT discharges from 3.33 volts to the lower threshold (set at 1/3 VREF or 1.67V for a typical 5.0V reference) sensed through RT1. The CLK signal is reset low when CT crosses the 1.67 volt threshold, turning off Q2 and turning on Q1, initiating another charge cycle.

The recommended value for CT is 1nF for frequencies in the 100 kHz or less range and smaller CT for higher frequencies. The minimum recommended values of RT1 and RT2 are 10 kΩ and 4.32 kΩ, respectively. Using these values maintains a ratio of at least 20:1 between the Rdsons of the internal FETs and the external timing resistors, resulting in minimal change in frequency over temperature. Because of the oscillator's susceptibility to capacitive coupling, examine the oscillator frequency by looking at the common RT1-RT2-CT node on the circuit board as opposed to looking at pins 3 and 4 directly. For good noise immunity, RT1 and RT2 should be placed as close to pins 3 and 4 of the IC as possible. CT should be returned directly to the ground pin of the IC with minimal

stray inductance and capacitance.

SYNCHRONIZATION

Both of the synchronization schemes shown in Figure 3 can be successfully implemented with the internal oscillator of the UCC3809. Both schemes allow access to the timing ramp needed for slope compensation and have minimal impact on the programmed maximum duty cycle. In the absence of a sync pulse, the PWM controller will run independently at the frequency set by RT1, RT2, and CT. This free running frequency must be approximately 15 to 20% lower than the sync pulse frequency to insure the free running oscillator does not cross the comparator threshold before the desired sync pulse.

Option I uses the synchronization pulse to pull pin 3 low, triggering the internal 1.67 V comparator to reset the RS latch and initiate a charging cycle. The valley voltage of the CT waveform is higher when synchronized using this configuration, decreasing the ramp charge and discharge times, thereby increasing the operating frequency; otherwise the overall shape of the CT voltage waveform is unchanged.

Option II uses the synchronization pulse to superimpose the sync voltage onto the peak of the CT waveform. This triggers the internal 3.33 V comparator, initiating a discharge cycle. The sync pulse is summed with the free running oscillator waveform at the CT node, resulting in a spike on top of the CT peak voltage.

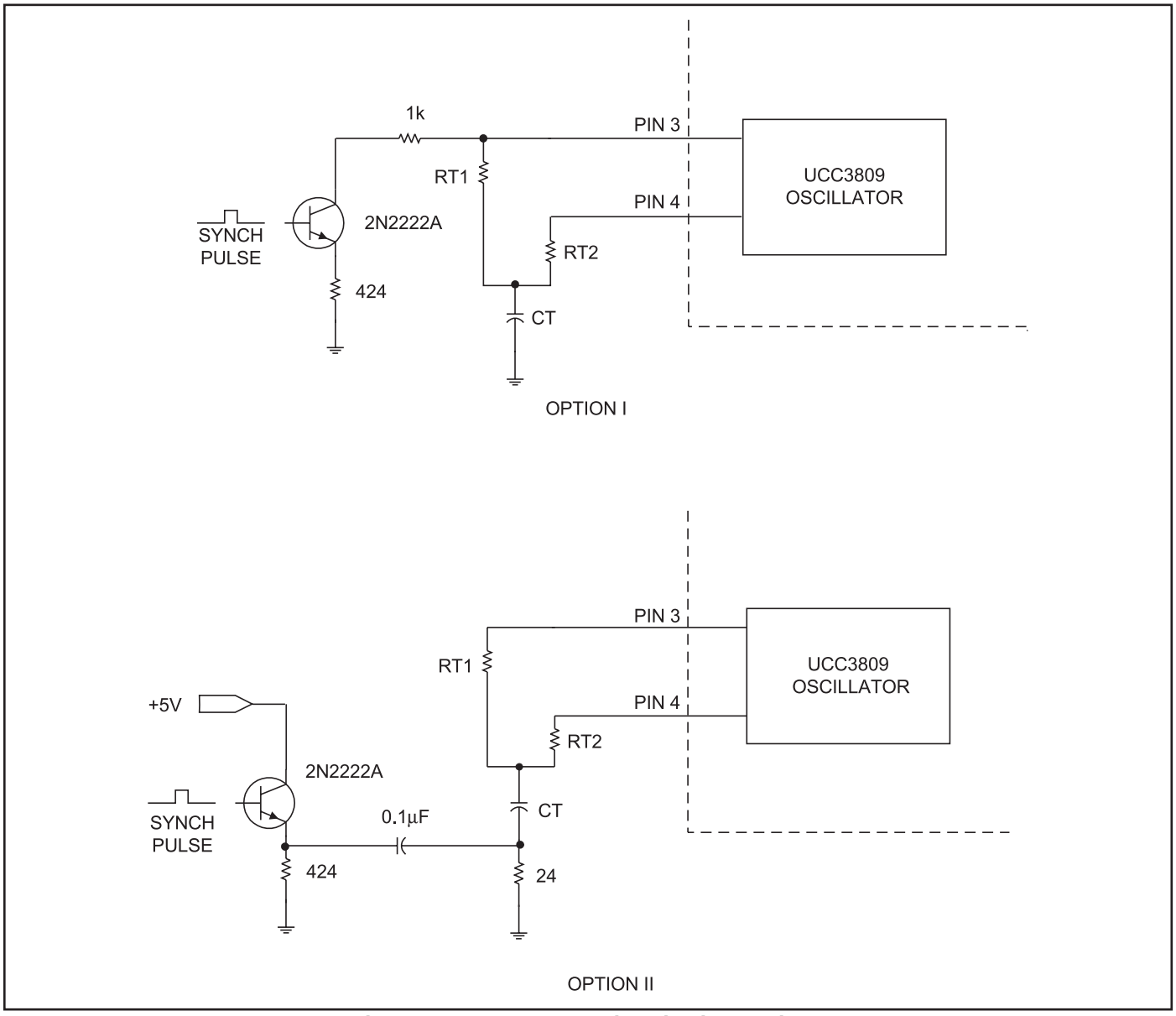


Figure 3. UCC3809 Synchronization Options

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460